

Serial No.: 10/720,173  
Docket No.: 102-1003  
Amendment dated July 27, 2006  
Reply to the Final Office Action of May 25, 2006

## **REMARKS**

### **Introduction**

Applicant notes with appreciation the Examiner's indication that claims 3, 5, 7, 12-18, 21-23 and 26-30 would be allowable if rewritten in independent form.

Upon entry of the present communication, claims 1-31 are pending in this application. No claims have been amended or cancelled. In view of the following remarks, reconsideration and allowance of all the pending claims are requested.

### **Rejection under 35 USC §102**

Claims 1, 4, 6, 8, 24-25, and 31 have been rejected under 35 U.S.C. §102(e) as being anticipated by the admitted prior art. Applicant traverses this rejection for at least the following reasons.

#### **1. Final Office Action of May 25, 2006**

At page 10 of the Final Office Action of May 25, 2006, the Examiner dissects the level shift unit 240 depicted in FIG. 6 to compare with the level shift unit 140 of FIG. 2 of the admitted prior art in an effort to prove that:

"figure 2 does perform some function of extending transient time, although the extent of this function may be minimal or even negligent when compared to the time extending characteristics of transient time extending part 243."

Then, on page 11 of the Final Office Action of May 25, 2006, the Examiner attempts to rely on a comparison between FIG. 4 and FIG. 7 in an effort to show that:

"Although it's hard to see because of the small size of the figures, there is a transient time extending element, although it's not as pronounced in effect as references 'D' and 'E' of figure 7."

Finally, the Examiner concludes by noting that:

"applicant has not really defined 'transient time' in the claimed invention" and that "it appears that the applicant is attempting to narrow the scope of the claimed invention by

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reading in the definition of 'transient time' as characterized by the specification."

Applicant respectfully addresses each one of the issues raised by the Examiner in the remarks that follow.

## 2. Definition of Transient Time

First, Applicant respectfully submits that "transient" as in "transient time" is a term that is well known in the art that refers to an amount of time taken to change between predetermined values or states. In this case, "transient time" is used to refer to output voltages. That is, the plain and ordinary meaning of "transient" and "transient time" would be readily appreciated by one of ordinary skill in the art without an explicit definition. Since the definition(s) of "transient" and/or "transient time" would be clear to one of ordinary skill in the art, especially within the context of the present invention, Applicant is not required to explicitly define these terms in the detailed description. Thus, contrary to the Examiner's assertion that "applicant is attempting to narrow the scope...by reading in the definition of 'transient time'...", Applicant is simply using the terms "transient" and "transient time" according to their proper and known meaning.

Furthermore, Applicant has described what is being referred by "transient time" in each one of the independent claims that is pending in this application. For example, independent claim 1 recites "a transient time...during which the potential level of the signal ... is converted from a first signal level to a second signal level and vice versa." This is a definition of transient time. Similarly, independent claim 6 recites "the transient time being a time period during which the level is converted from a first signal level to a second signal level and vice versa." This is also a definition of transient time. In independent claim 8, "a first transient time, during which a level of the first nozzle selection signal is changed between first and second levels" defines a transient time. Finally, independent claim 31 recites "increase a time required to change an output thereof between the logic high and the logic low." This is also a transient time. Thus, it is evident that Applicant is not only relying on the well-known definition of transient and transient time, but is also relying on "transient time," as defined in the explicit language of the claims of the invention. Accordingly, the Examiner's position with respect to "transient time" allegedly not being defined is not supported.

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3. An Extension of Transient Time is Not Inherent

Furthermore, without explicitly stating, the Examiner appears to rely on a theory of inherency in an effort to show that the buffer 144 of the admitted prior art of FIG. 2 anticipates Applicant's "at least one time extending element to extend...a transient time," as recited in independent claim 1 and other similar elements of other independent claims. For example, on page 10 of the Final Office Action of May 25, 2006 the Examiner states that "figure 2 does perform some function of extending transient time, although the extent of this function may be minimal or even negligent when compared to the time extending characteristics of transient time extending part 243." However, it remains unclear why this conclusion would necessarily follow from the Examiner's component by component comparison of the buffer 140 of the admitted prior art of FIG. 2 with the time extending part 243 of FIG. 6. Specifically, the Examiner has not provided any evidence or technical reasoning to support the conclusion that an inverter INV2 (i.e., "the right part of the buffer 144" referred to by the Examiner in the Final Office Action) would necessarily extend a transient time. It is also unclear how the Examiner is determining that there is some measure of "minimal or even negligent" extension of transient time caused by INV2 of the buffer 140 of the admitted prior art of FIG. 2, since minimal or negligible effects on voltage signals are typically difficult to measure let alone determine from a circuit diagram in a paper publication.

In the event that the Office Action is relying on the theory of inherency in any manner, "the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). See also MPEP 2112. Accordingly, since the Examiner has not provided a basis in fact or technical reasoning as to reasonably determine that the buffer 140 of the admitted prior art inherently would extend a transient time, the Examiner's application of the inherency principle here is improper.

4. Comparison of Figure 7 of the Specification with Figure 4 of the Admitted Prior Art

Applicant further submits that the Examiner's interpretation of FIGS. 4 and 7 actually contradicts the Examiner's position, since the distinction between the admitted prior art of FIG. 2

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and the claims of Applicant's invention is further clarified by a proper comparison between FIG. 4 of the admitted prior art and FIG. 7 of Applicant's specification.

More particularly, FIG. 2 of the admitted prior art shows that the voltage (A) input to the buffer 144, which the Examiner equates with Applicant's "time extending element," is converted to the voltage output (B) by the buffer 144. However, FIG. 4 clearly shows that when the input voltage (A) is changed from low to high, the transient time (i.e., the amount of time taken to change between low voltage and high voltage and vice versa) is identical to the transient time of the output voltage (B), which also changes according to the input voltage (A). In other words, the amount of time it takes the voltage (A) (i.e., input to the buffer 144) to change is the same as the amount of time it takes the voltage (B) (i.e., output from the buffer 144) to change in FIG. 4 of the admitted prior art. This is evidenced by a width (i.e., a duration) of each transient time of voltage (A) and voltage (B) in FIG. 4. Thus, the buffer 144 of the admitted prior art cannot be interpreted as extending a transient time of the level converter 142 and/or the level shift unit 140 of the admitted prior art.

Stated differently, assuming for the sake of argument that the buffer 144 did extend the transient time of the level converter 142, then the transient time of the voltage (B) would have to be wider (i.e., longer in duration) than the transient time of the voltage (A), as illustrated in FIG. 4 of the admitted prior art. However, this is clearly not the case. Instead, FIG. 4 illustrates that the amount of time taken for the voltage (A) to change between the low voltage and high voltage is the same as the amount of time taken for the voltage (B) to change between the low voltage and high voltage, and vice versa. Thus, as set forth in Applicant's Remarks filed March 16, 2006, the buffer 144 (and/or the INV2) merely delays the output, but does not extend the "transient time during which the potential level of the signal inputted from the level converter to the switching unit is converted from a first signal level to a second signal level and vice versa," as recited in independent claim 1 of Applicant's invention.

On the other hand, FIG. 7 of Applicant's specification illustrates various voltage levels of voltages in the level shift unit 240 of FIG. 6. In particular, FIG. 7 includes voltage (A), which is input to the transient time extending part 243 of FIG. 6 and voltage (B), which is output from the transient time extending part 243 of FIG. 6. It is evident from FIG. 7 that the voltage (B) shown

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in FIG. 7 has a transient time that is greater than the transient time of the voltage (A) by an amount of time that corresponds to "D" and/or "E." Thus, unlike the admitted prior art of FIGS. 2 and 4, the transient time of the voltage (A) output from the level converter 241 has been extended by the transient time extending part 243 to the transient time of the voltage (B). Accordingly, Applicant respectfully submits that, contrary to the Examiner's assertions, neither the buffer 144 of the admitted prior art of FIG. 2, the INV2 of the admitted prior art of FIG. 2, nor a combination thereof extends a transient time "during which the potential level of the signal inputted from the level converter to the switching unit is converted from a first signal level to a second signal level and vice versa," as recited in independent claim 1 of Applicant's invention. Accordingly, the admitted prior art does not anticipate independent claim 1 of Applicant's invention.

For at least the same reasons, the buffer 140 of the admitted prior art does not "extend[ing] a transient time by a predetermined time in accordance with an output signal generating when the level of the inputted signal is converted, the transient time being a time period during which the level is converted from a first signal level to a second signal level and vice versa," as recited in independent claim 6 of Applicant's invention. Accordingly, the admitted prior art does not anticipate independent claim 6 of Applicant's invention.

Nor can any component of the admitted prior art of FIG. 2 be interpreted as "a level shift unit generating a first nozzle selection signal having a first transient time, during which a level of the first nozzle selection signal is changed between first and second levels, in response to the control nozzle selection signal, and generating a second nozzle selection signal having a second transient time extended by a period from the first transient time," as recited in independent claim 8 of Applicant's invention. Accordingly, the admitted prior art does not anticipate independent claim 8 of Applicant's invention.

Similarly, the admitted prior art of FIG. 2 does not disclose "a level shift unit to convert the nozzle selection signal to have a predetermined level to drive the heating element between a logic high and a logic low and having one or more logic units to increase a time required to change an output thereof between the logic high and the logic low," as recited in independent claim 31 of Applicant's invention. Accordingly, the admitted prior art does not anticipate

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independent claim 31 of Applicant's invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "The elements must be arranged as required by the claim..." In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Further, in the event that the Office Action is relying on the theory of inherency in any manner, "the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). See also MPEP 2112. Accordingly, since the admitted prior art does not explicitly or inherently teach every element as recited in independent claims 1, 6, 8, and 31, the admitted prior art cannot be properly used to reject independent claims 1, 6, 8, and 31 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claims 1, 6, 8, and 31 are allowable over the admitted prior art, and withdrawal of this rejection and allowance of these claims are earnestly solicited.

Regarding claims 4 and 24-25, it is respectfully submitted that for at least the reason that claims 4 and 24-25 depend from independent claims 1 and 8, respectively, and therefore contain each of the features as recited in these claims, claims 4 and 24-25 are therefore also patentable over the admitted prior art, and withdrawal of the rejection of these claims and allowance thereof are earnestly solicited.

### **Rejection under 35 USC §103**

Claims 2, 9-11 and 19-20 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in view of U.S. Patent No. 6,273,537 to Hiwada. Applicant traverses this rejection for at least the following reasons.

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Claims 2, 9-11, and 19-20 depend from allowable independent claims 1 and 8, respectively, and therefore include each of the features of these claims. The Examiner acknowledges that the admitted prior art does not disclose the features of claims 2, 9-11, and 19-20. See Office Action of May 25, 2006 page 9. However, the Examiner relies on Hiwada as allegedly teaching the features that the admitted prior art lacks. See Office Action of May 25, 2006 page 9. Applicant respectfully submits that even if Hiwada does in fact teach the features of these dependent claims, as alleged by the Examiner, the admitted prior art and Hiwada, either separately or in combination with one another, fail to teach or suggest "a level shift unit having a level converter converting a potential level of a signal inputted therein into a predetermined potential level to drive the switching unit, and a transient time extending part provided with at least one time extending element to extend by a predetermined time a transient time during which the potential level of the signal inputted from the level converter to the switching unit is converted from a first signal level to a second signal level and vice versa," as recited in independent claim 1, and "a level shift unit generating a first nozzle selection signal having a first transient time, during which a level of the first nozzle selection signal is changed between first and second levels, in response to the control nozzle selection signal, and generating a second nozzle selection signal having a second transient time extended by a period from the first transient time," as recited in independent claim 8 of Applicant's invention. Accordingly, claims 2, 9-11, and 19-20 are patentable over the references relied upon by the Examiner at least by virtue of their dependency on independent claims 1 and 8, respectively, and withdrawal of the rejection and allowance of these claims are earnestly solicited.

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**Conclusion**

It is respectfully submitted that a full and complete response has been made to the outstanding Office Action and, as such, there being no other objections or rejections, this application is in condition for allowance, and a notice to this effect is earnestly solicited.


If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

If any further fees are required in connection with the filing of this amendment, please charge the same to our Deposit Account No. 502827.

Respectfully submitted,

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